

WHAT IS CLAIMED IS:

1. A modulator that receives a digital baseband signal and modulates the digital baseband signal to a quadrature modulated output signal, the modulator comprising:

5 a quadrature modulator compensation signal processor (QMCSP) adapted to receive the digital baseband signal, where the QMCSP includes a first digital filter to generate a digital compensated signal so that the digital compensated signal negates at least a portion of a quadrature impairment in an analog quadrature modulator system (AQMS) for a plurality of baseband frequencies;

10 the AQMS, where the AQMS is adapted to receive the digital compensated signal and a local oscillator signal, where the AQMS is further adapted to quadrature modulate, in analog domain, the digital compensated signal to the quadrature modulated output signal;

15 a termination switch adapted to provide an observation signal, where the termination switch is coupled to a sample signal related to the quadrature modulated output signal and coupled to a source for a ground signal, where the termination switch further switches between the sample signal and the source for the ground signal in response to a ground switch control signal;

20 a variable phase shifter adapted to receive the local oscillator signal and to provide a phase shifted output signal, where the phase shifted output signal is selectable to at least 3 phase shifts, and where a phase shift is selected in response to a phase shifter control signal;

25 an analog quadrature demodulator system (AQDS) adapted to receive the observation signal and the phase shifted output signal, the AQDS adapted to demodulate the observation signal and to recover a received baseband signal that is related to the baseband signal, and where the received baseband signal includes quadrature impairment;

30 a quadrature demodulator compensation signal processor (QDCSP) adapted to receive the received baseband signal from the AQDS, where the QDCSP includes a second digital filter to generate a demodulated baseband

signal such that at least a portion of the quadrature impairment added to the received baseband signal by the AQDS is compensated in the demodulated baseband signal for a plurality of frequencies; and

an adaptive control processing and compensation estimation (ACPCE) circuit adapted to monitor the baseband signal and the received baseband signal, where the ACPCE circuit is further adapted to update parameters used by the QMCSP and the QDCSP to compensate for quadrature impairment.

2. The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate a first in-phase portion of the digital compensated signal;

a second FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second in-phase portion of the digital compensated signal;

a third FIR filter adapted to receive an in-phase portion of the baseband signal and to generate a first quadrature-phase portion of the digital compensated signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second quadrature-phase portion of the digital compensated signal;

a first summing circuit adapted to combine the first in-phase portion of the digital compensated signal with the second in-phase portion of the digital compensated signal to generate an in-phase digital compensated signal; and

a second summing circuit adapted to combine the first quadrature-phase portion of the digital compensated signal with the second quadrature-phase portion of the digital compensated signal to generate a quadrature-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

3. The modulator as defined in Claim 2, wherein the first digital filter of the QMCSP further comprises:

a first register adapted to store a first value, and where the first summing circuit is further configured to combine the first value with the first and the second in-phase portions of the digital compensated signal to generate the in-phase portion of the digital compensated signal; and

a second register adapted to store a second value, and where the second summing circuit is further configured to combine the second value with the first and the second quadrature-phase portions of the digital compensated signal to generate the quadrature-phase portion of the digital compensated signal.

4. The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate an in-phase digital compensated signal;

a second FIR filter adapted to receive an in-phase portion of the baseband signal and to generate a first quadrature-phase portion of the digital compensated signal;

a third FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second quadrature-phase portion of the digital compensated signal; and

a summing circuit adapted to combine the first quadrature-phase portion of the digital compensated signal with the second quadrature-phase portion of the digital compensated signal to generate a quadrature-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

5. The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate a first in-phase portion of the digital compensated signal;

a second FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second in-phase portion of the digital compensated signal;

a third FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a quadrature-phase digital compensated signal; and

a summing circuit adapted to combine the first in-phase portion of the digital compensated signal with the second in-phase portion of the digital compensated signal to generate an in-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

6. The modulator as defined in Claim 1, wherein the QDCSP is implemented in firmware.

7. The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

a second FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

5 a first summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal; and

10 a second summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

15 8. The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first register adapted to store a first value that is related to a DC offset in an in-phase portion of the received baseband signal;

a second register adapted to store a second value that is related to a DC offset in a quadrature-phase portion of the received baseband signal;

20 a first summing circuit adapted to combine the first value with the in-phase portion of the received baseband signal to produce an in-phase portion of a reduced offset received baseband signal;

25 a second summing circuit adapted to combine the second value with the quadrature-phase portion of the received baseband signal to produce a quadrature-phase portion of the reduced offset received baseband signal;

a first FIR filter adapted to receive the in-phase portion of the reduced offset received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

30 a second FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive a in-phase portion of the reduced offset received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

a third summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal; and

a fourth summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

9. The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate an in-phase demodulated baseband signal;

a second FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

a summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the

quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

10. The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

5 a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

10 a second FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a quadrature-phase demodulated baseband signal; and

15 a summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

20 11. The modulator as defined in Claim 1, further comprising a coupler adapted to provide the sample signal from an output of a radio frequency amplifier, where the quadrature modulated output signal is applied as an input to the radio frequency amplifier.

12. The modulator as defined in Claim 1, further comprising a coupler adapted to provide the sample signal from the quadrature modulated output signal.

25 13. The modulator as defined in Claim 1, where the ACPCE circuit is configured to monitor the baseband signal and the received baseband signals in short bursts of time between about 50 microseconds to about 200 microseconds, and is further configured to store the monitored signals in a memory device.

30 14. The modulator as defined in Claim 1, wherein the local oscillator frequency is radio frequency (RF).

15. The modulator as defined in Claim 1, wherein the local oscillator frequency is intermediate frequency (IF).

16. The modulator as defined in Claim 15, further comprising a frequency upconverter adapted to receive a signal as an input that includes the quadrature modulated output signal, and to mix the signal with an RF signal.

17. The modulator as defined in Claim 1, wherein the ground signal switched by the termination switch is alternating current (AC) coupled to ground.

18. The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to provide a test signal, and the QMCSP is configured to accept the test signal, and where the test signal includes test tones that enable the QDCSP to detect quadrature impairment characteristics.

19. The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to provide updates to the first digital filter and to the second digital filter through state parameter vectors to the QMCSP and the QDCSP, respectively, to update instructions that negate the quadrature impairment.

20. The modulator as defined in Claim 19, wherein the QMCSP is adapted to activate the updates substantially simultaneously.

21. The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to activate the phase shifter control signal to select the phase shift of the phase shifted output signal to measure quadrature impairment characteristics of the AQMS and the AQDS.

22. The modulator as defined in Claim 21, wherein the ACPCE circuit is configured to activate the ground switch control to characterize a DC offset corresponding to a selected phase shift.

23. The modulator as defined in Claim 1, wherein the AQDS is further coupled to a receive path from an antenna to receive a transmitted signal from an external transmitter so that the AQDS demodulates the transmitted signal.

24. A circuit that compensates for gain and phase imbalance at multiple frequencies in an analog quadrature modulator, the circuit comprising:

a quadrature modulator compensation signal processor (QMCSP) adapted to receive a first signal and to generate a second signal, where the

second signal negates at least a portion of a first quadrature impairment over a plurality of frequencies in a third signal that is introduced by an analog quadrature modulator;

5 a data acquisition memory adapted to store at least a first real time burst of the first signal, and to store a second real time burst of a fourth signal that is quadrature demodulated and converted to digital from a signal related to the third signal, where the fourth signal includes a second quadrature impairment introduced by an analog quadrature demodulator; and

10 a quadrature demodulator compensation signal processor (QDCSP) adapted to retrieve at least a portion of the stored burst of the fourth signal from the data acquisition memory and to generate a demodulated data such that the demodulated data is substantially free of quadrature impairment introduced by the analog quadrature demodulator.

15 25. The circuit as defined in Claim 24, wherein the real time bursts are between about 50 microseconds to about 200 microseconds long.

20 26. The circuit as defined in Claim 24, further comprising an adaptive control processing and compensation estimation (ACPCE) circuit adapted to monitor the first signal and the demodulated data, where the ACPCE is configured to activate a ground switch control and a phase shifter control to analyze quadrature impairment characteristics, and where the ACPCE is configured to calculate parameters used by the QMCSP and the QDCSP to compensate for quadrature impairment.

27. The circuit as defined in Claim 26, wherein the ACPCE is configured to analyze samples of the first signal that are delayed in time relative to samples of the third signal.

25 28. The circuit as defined in Claim 26, wherein the ACPCE is configured to provide an activation signal to the QMCSP that activates the compensation parameters calculated and loaded by the ACPCE at substantially the same time.

29. The circuit as defined in Claim 24, wherein the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the first signal and to generate a first in-phase portion of the second signal;

a second FIR filter adapted to receive a quadrature-phase portion of the first signal and to generate a second in-phase portion of the second signal;

a third FIR filter adapted to receive an in-phase portion of the first signal and to generate a first quadrature-phase portion of the second signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the first signal and to generate a second quadrature-phase portion of the second signal;

a first summing circuit adapted to combine the first in-phase portion of the second signal with the second in-phase portion of the second signal to generate an in-phase second signal; and

a second summing circuit adapted to combine the first quadrature-phase portion of the second signal with the second quadrature-phase portion of the second signal to generate a quadrature-phase second signal, where the in-phase second signal and the quadrature-phase second signal comprise the second signal.

30. The circuit as defined in Claim 29, wherein the QMCSP further comprises:

a first register adapted to store a first value, and where the first summing circuit is further configured to combine the first value with the first and the second in-phase portions of the second signal to generate the in-phase second signal; and

a second register adapted to store a second value, and where the second summing circuit is further configured to combine the second value with the first and the second quadrature-phase portions of the second signal to generate the in-phase second signal.

31. The circuit as defined in Claim 24, wherein the QDCSP further comprises:

a first register adapted to store a first value related to a DC offset in an in-phase portion of the received baseband signal;

5 a second register adapted to store a second value related to a DC offset in a quadrature-phase portion of the received baseband signal;

a first summing circuit adapted to combine the first value with the in-phase portion of the received baseband signal to produce an in-phase portion of a reduced offset received baseband signal;

10 a second summing circuit adapted to combine the second value with the quadrature-phase portion of the received baseband signal to produce a quadrature-phase portion of the reduced offset received baseband signal;

15 a first FIR filter adapted to receive the in-phase portion of the reduced offset received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

a second FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

20 a third FIR filter adapted to receive a in-phase portion of the reduced offset received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

25 a third summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal; and

30 a fourth summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase

demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

5 32. A quadrature modulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, in order to compensate for gain and phase imbalance in a quadrature modulator in a plurality of frequencies, comprising:

a first digital filter adapted to receive an in-phase portion of the input signal and to generate a first in-phase portion of the output signal;

10 a second digital filter adapted to receive a quadrature-phase portion of the input signal and to generate a second in-phase portion of the output signal;

a third digital filter adapted to receive an in-phase portion of the input signal and to generate a first quadrature-phase portion of the output signal;

15 a fourth digital filter adapted to receive a quadrature-phase portion of the input signal and to generate a second quadrature-phase portion of the output signal;

a first summing circuit adapted to combine the first and the second in-phase portions of the output signal to generate the in-phase output signal; and

20 a second summing circuit adapted to combine the first and the second quadrature-phase portions of the output signal to generate the quadrature-phase output signal.

33. The quadrature modulation compensation signal processor as defined in Claim 32, wherein the first, the second, the third, and the fourth digital filters comprise finite impulse response (FIR) filters.

25 34. The quadrature modulation compensation signal processor as defined in Claim 32, further comprising:

a first register adapted to maintain a first value;

a second register adapted to maintain a second value;

30 wherein the in-phase summing circuit is further adapted to combine the first value to generate the in-phase output signal; and

wherein the quadrature-phase summing circuit is further adapted to combine the second value to generate the quadrature-phase output signal.

35. A quadrature modulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, in order to compensate for gain and phase imbalance in a quadrature modulator in a plurality of frequencies, comprising:

a first digital filter adapted to receive an in-phase portion of the input signal and to generate the in-phase output signal;

a second digital filter adapted to receive an in-phase portion of the input signal and to generate a first quadrature-phase portion of the output signal;

a third digital filter adapted to receive a quadrature-phase portion of the input signal and to generate a second quadrature-phase portion of the output signal; and

a quadrature-phase summing circuit adapted to combine the first quadrature-phase portion of the output signal and the second quadrature-phase portion of the output signal to generate the quadrature-phase output signal.

36. The quadrature modulation compensation signal processor as defined in Claim 35, wherein the first, the second, and the third digital filters comprise finite impulse response (FIR) filters.

37. The quadrature modulation compensation signal processor as defined in Claim 35, further comprising:

a first register adapted to maintain a first value;

a second register adapted to maintain a second value;

an in-phase summing circuit adapted to combine the first value to generate the in-phase output signal; and

wherein the quadrature-phase summing circuit is further adapted to combine the second value to generate the quadrature-phase output signal.

38. A quadrature modulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, in order to compensate for gain and phase imbalance in a quadrature modulator in a plurality of frequencies, comprising:

5 a first digital filter adapted to receive an in-phase portion of the input signal and to generate a first in-phase portion of the output signal;

a second digital filter adapted to receive a quadrature-phase portion of the input signal and to generate a second in-phase portion of the output signal;

10 a third digital filter adapted to receive a quadrature-phase portion of the input signal and to generate the quadrature-phase output signal; and

an in-phase summing circuit adapted to combine the first in-phase portion of the output signal and the second in-phase portion of the output signal to generate the in-phase output signal.

39. The quadrature modulation compensation signal processor as defined in Claim 38, wherein the first, the second, and the third digital filters comprise finite impulse response (FIR) filters.

40. The quadrature modulation compensation signal processor as defined in Claim 38, further comprising:

20 a first register adapted to maintain a first value;

a second register adapted to maintain a second value;

a quadrature-phase summing circuit adapted to further combine the second value to generate the quadrature-phase output signal; and

wherein the in-phase summing circuit is further adapted to combine the first value to generate the in-phase output signal.

41. A quadrature demodulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, to at least partially compensate for gain and phase imbalance in the input signal over a plurality of frequencies, where the gain and phase imbalance is introduced by a quadrature demodulator, comprising:

30 a first register adapted to store a first value related to a DC offset in an in-phase portion of the input signal;

a second register adapted to store a second value related to a DC offset in a quadrature-phase portion of the input signal;

a first summing circuit adapted to combine the first value with the in-phase portion of the input signal to produce an in-phase portion of a first signal;

5 a second summing circuit adapted to combine the second value with the quadrature-phase portion of the input signal to produce a quadrature-phase portion of the first signal;

a first digital filter adapted to receive the in-phase portion of the first signal and to generate a first in-phase portion of the output signal;

10 a second digital filter adapted to receive the quadrature-phase portion of the first signal and to generate a second in-phase portion of the output signal;

a third digital filter adapted to receive the in-phase portion of the first signal and to generate a first quadrature-phase portion of the output signal;

15 a fourth digital filter adapted to receive the quadrature-phase portion of the first signal and to generate a second quadrature-phase portion of the output signal;

a third summing circuit adapted to combine the first in-phase portion of the output signal with the second in-phase portion of the output signal to generate the in-phase output signal; and

20 a fourth summing circuit adapted to combine the first quadrature-phase portion of the output signal with the second quadrature-phase portion of the output signal to generate the quadrature-phase output signal.

42. The quadrature demodulation compensation signal processor as defined in Claim 41, wherein the first, the second, the third, and the fourth digital filters
25 comprise finite impulse response (FIR) filters.

43. A quadrature demodulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, to at least partially compensate for gain and phase imbalance in the input signal over a plurality of frequencies, where the gain and phase imbalance is introduced by a quadrature demodulator, comprising:

- a first register adapted to store a first value related to a DC offset in an in-phase portion of the input signal;
- a second register adapted to store a second value related to a DC offset in a quadrature-phase portion of the input signal;
- a first summing circuit adapted to combine the first value with the in-phase portion of the input signal to produce an in-phase portion of a first signal;
- a second summing circuit adapted to combine the second value with the quadrature-phase portion of the input signal to produce a quadrature-phase portion of the first signal;
- a first digital filter adapted to receive the in-phase portion of the first signal and to generate the in-phase output signal;
- a second digital filter adapted to receive the in-phase portion of the first signal and to generate a first quadrature-phase portion of the output signal;
- a third digital filter adapted to receive the quadrature-phase portion of the first signal and to generate a second quadrature-phase portion of the output signal; and
- a third summing circuit adapted to combine the first quadrature-phase portion of the output signal with the second quadrature-phase portion of the output signal to generate the quadrature-phase output signal.

44. The quadrature demodulation compensation signal processor as defined in Claim 43, wherein the first, the second, and the third digital filters comprise finite impulse response (FIR) filters.

45. A quadrature demodulation compensation signal processor that converts an input signal to an output signal, where the output signal includes an in-phase output signal and a quadrature-phase output signal, to at least partially compensate for gain and

phase imbalance in the input signal over a plurality of frequencies, where the gain and phase imbalance is introduced by a quadrature demodulator, comprising:

a first register adapted to store a first value related to a DC offset in an in-phase portion of the input signal;

5 a second register adapted to store a second value related to a DC offset in a quadrature-phase portion of the input signal;

a first summing circuit adapted to combine the first value with the in-phase portion of the input signal to produce an in-phase portion of a first signal;

10 a second summing circuit adapted to combine the second value with the quadrature-phase portion of the input signal to produce a quadrature-phase portion of the first signal;

a first digital filter adapted to receive the in-phase portion of the first signal and to generate a first in-phase portion of the output signal;

15 a second digital filter adapted to receive the quadrature-phase portion of the first signal and to generate a second in-phase portion of the output signal;

a third digital filter adapted to receive the quadrature-phase portion of the first signal and to generate the quadrature-phase output signal; and

20 a third summing circuit adapted to combine the first in-phase portion of the output signal with the second in-phase portion of the output signal to generate the in-phase output signal.

46. The quadrature demodulation compensation signal processor as defined in Claim 45, wherein the first, the second, and the third digital filters comprise finite impulse response (FIR) filters.

25 47. A variable phase shifter that receives an oscillator signal and provides an output signal where, in response to a control signal, a phase of the output signal is selectable to at least 3 phases, the variable phase shifter comprising:

a plurality of paths adapted to carry the oscillator signal, where a path in the plurality of paths has a first end and a second end, where the plurality of paths include paths of varying lengths;

a first switch coupled to the oscillator signal and to the first ends of the plurality of paths, where the first switch is configured to select a path in the plurality of paths in response to the control signal; and

5 a second switch adapted to provide the output signal, where the second switch is coupled to the second ends of the plurality of paths, where the second switch is configured to select the same path in the plurality of paths selected by the first switch in response to the control signal.

48. The variable phase shifter as defined in Claim 47, wherein the lengths of the paths are selected so that, at a frequency of the oscillator signal, a difference in
10 phase when a first path from the plurality of paths is selected and when a second path from the plurality of paths is selected conforms to about 180 degrees divided by N , where N conforms to a count of the plurality of paths.

49. The variable phase shifter as defined in Claim 47, wherein the lengths of the paths range from about 2 centimeters to about 5 centimeters.

15 50. A method of quadrature modulating baseband signals comprising:
receiving an input signal in digital form, where the input signal includes both an in-phase portion and a quadrature-phase portion;

applying a first time-domain impulse response to the input signal to convert the input signal to a digital compensated signal, where the digital
20 compensated signal substantially negates a quadrature impairment associated with a forward modulation path;

converting the digital compensated signal from digital to an analog version;

quadrature modulating, in an analog quadrature modulator, the analog
25 version of the digital compensated signal to a quadrature modulated signal;

receiving a sample signal of the quadrature modulated signal;

applying the sample signal as an input to an analog quadrature demodulator and quadrature demodulating the sample signal to a quadrature demodulated sample signal;

30 converting the quadrature demodulated sample signal from analog to a digital version;

54. The method as defined in Claim 50, further comprising:
detecting an absence of transmission by an RF amplifier associated with
the input signal;

5 receiving an external signal transmitted by an external transmitter; and
applying the external signal as an input to the analog quadrature
demodulator and demodulating the external signal.

55. The method as defined in Claim 50, further comprising:
compensating for a DC offset associated with the forward modulation
path by combining the digital compensated signal with a first calculated DC
offset; and

10 compensating for a DC offset associated with the reverse demodulation
path by combining the received baseband signal with a second calculated DC
offset.

56. A method of digitally filtering a first signal that includes an in-phase
15 portion and a quadrature-phase portion to a second signal that also includes an in-phase
portion and a quadrature phase portion, the method comprising:

applying a first impulse response to the in-phase portion of the first
signal to produce an II signal;

20 applying a second impulse response to the quadrature-phase portion of
the first signal to produce a QI signal;

applying a third impulse response to the in-phase portion of the first
signal to produce an IQ signal;

applying a fourth impulse response to the quadrature-phase portion of the
first signal to produce a QQ signal;

25 combining the II signal and the QI signal to produce the in-phase portion
of the second signal; and

combining the IQ signal and the QQ signal to produce the quadrature-
phase portion of the second signal.

57. The method as defined in Claim 56, further comprising combining the
30 in-phase and the quadrature-phase portions of the second signal with DC offsets to
compensate for DC offset associated with a downstream process.

58. The method as defined in Claim 56, further comprising combining the in-phase and the quadrature-phase portions of the first signal prior to application of the digital filter with DC offsets to compensate for DC offsets associated with an upstream process.

5 59. A method of digitally filtering a first signal that includes an in-phase portion and a quadrature-phase portion to a second signal that also includes an in-phase portion and a quadrature phase portion, the method comprising:

applying a first impulse response to the in-phase portion of the first signal to produce the in-phase portion of the second signal;

10 applying a second impulse response to the in-phase portion of the first signal to produce an IQ signal;

applying a third impulse response to the quadrature-phase portion of the first signal to produce a QQ signal; and

15 combining the IQ signal and the QQ signal to produce the quadrature-phase portion of the second signal.

60. A method of digitally filtering a first signal that includes an in-phase portion and a quadrature-phase portion to a second signal that also includes an in-phase portion and a quadrature phase portion, the method comprising:

20 applying a first impulse response to the in-phase portion of the first signal to produce an II signal;

applying a second impulse response to the quadrature-phase portion of the first signal to produce a QI signal;

applying a third impulse response to the quadrature-phase portion of the first signal to produce the quadrature-phase portion of the second signal; and

25 combining the II signal and the QI signal to produce the in-phase portion of the second signal.

61. A method of determining time domain impulse responses that complement gain and phase imbalance in a quadrature modulator, the method comprising:

30 receiving and storing at least a portion of an input signal in a memory;

receiving and storing at least a portion of a demodulated baseband signal in the memory;

analyzing the at least portions of the input signal and the demodulated baseband signal;

5 characterizing the quadrature impairment characteristics of an analog quadrature modulator system and an analog quadrature demodulator system in frequency domain by computing a first set of transfer functions of the quadrature impairments;

10 computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises an inverse system response to the first set of transfer functions;

converting a first portion of the second set of transfer functions to a first set of time domain impulse responses that substantially negates the gain and phase imbalance in the analog quadrature modulator system; and

15 converting a second portion of the second set of transfer functions to a second set of time domain impulse responses that substantially negates the gain and phase imbalance in the analog quadrature demodulator system.

62. The method as defined in Claim 61, further comprising phase shifting a local oscillator signal to the analog quadrature demodulator system to characterize the first set and the second set of transfer functions.

63. The method as defined in Claim 62, further comprising:

applying the first set of time domain impulse responses to the input signal in real time;

25 applying the second set of time domain impulse responses to the demodulated baseband signal;

comparing time shifted samples of the input signal with samples of the demodulated baseband signal and generating an error indication of quadrature impairment compensation; and

30 adjusting the first set and the second set of time domain impulse responses to reduce a magnitude of the error indication.

64. A method of at least partially compensating for gain and phase imbalance in an analog quadrature modulator system (AQMS), the method comprising:

applying test signals that include a plurality of baseband frequencies to a forward path of the AQMS;

5 detecting an envelope of an output signal of the AQMS;

storing at least a portion of the envelope of the output signal in a memory;

relating the at least portion of the envelope to the applied test signals;

10 characterizing the gain and phase imbalance of the AQMS in frequency domain by computing a first set of transfer functions of the quadrature impairment characteristics;

computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises an inverse system response to the first set of transfer functions;

15 converting a first portion of the second set of transfer functions to time domain impulse responses that substantially negate the gain and phase imbalance in the AQMS; and

applying the time domain impulse responses to input signals in the forward path of the AQMS.

20 65. A method of at least partially compensating for gain and phase imbalance in an analog quadrature modulator system (AQMS), the method comprising:

digitally demodulating a signal related to an output of the AQMS in a digital quadrature demodulator;

25 characterizing the gain and phase imbalance of the AQMS in frequency domain by computing a first set of transfer functions of the quadrature impairment characteristics;

computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises an inverse system response to the first set of transfer functions;

converting a first portion of the second set of transfer functions to time domain impulse responses that substantially negate the gain and phase imbalance in the AQMS; and

5 applying the time domain impulse responses to input signals in the forward path of the AQMS.

66. A method of distinguishing gain and phase imbalance produced by an analog quadrature modulator system (AQMS) from gain and phase imbalance produced by an analog quadrature demodulator system (AQDS), the method comprising:

- 10 (a) selecting a first phase shifted version of a local oscillator signal;
- (b) applying the first phase shifted version of the local oscillator signal as an input to the AQDS;
- (c) monitoring and storing at least a portion of a first signal that is upstream of the AQMS;
- 15 (d) monitoring and storing at least a portion of a second signal that is downstream of the AQDS;
- (e) selecting and applying a second phase shifted version of the local oscillator signal as an input to the AQDS;
- (f) repeating (c) and (d);
- (g) selecting and applying a third phase shifted version of the local oscillator signal as an input to the AQDS;
- 20 (h) repeating (c) and (d); and
- (i) computing a frequency domain transfer function of the AQMS and the AQDS gain and phase imbalances.

25 67. The method as defined in Claim 66, wherein the first, the second, and the third phase shifted versions are selected by selecting a first, a second, and a third paths, respectively, interspersed between a source for the local oscillator signal and the input to the AQDS.

68. A method of distinguishing gain and phase imbalance produced by an analog quadrature modulator system (AQMS) from gain and phase imbalance produced by an analog quadrature demodulator system (AQDS), the method comprising:

5 selectively applying at least three phase shifted versions of a local oscillator signal as an input to the AQDS;

monitoring and storing at least a portion of a first signal that is upstream of the AQMS and at least a portion of a second signal that is downstream of the AQDS for at least three of the phase shifted versions selected; and

10 computing a frequency domain transfer function of the AQMS and the AQDS gain and phase imbalances.

69. The method as defined in Claim 68, wherein a phase shift between the at least three phase shifted versions is approximately 180 degrees divided by N , where N is the number of phase shifted versions applied as an input to the AQDS.

70. A method of distinguishing DC offsets produced by an analog quadrature modulator system (AQMS) from DC offsets produced by an analog quadrature demodulator system (AQDS) for a plurality frequencies of a local oscillator signal comprising:

15 detecting a change in a frequency of the local oscillator signal, where the local oscillator signal is applied as a first input to the AQDS;

20 activating a termination switch such that a ground signal is applied as a second input to the AQDS;

detecting a first DC offset in an output signal of the AQDS, where the first DC offset is related to the DC offset produced by the AQDS;

25 deactivating the termination switch such that a signal related to an output of the AQMS is applied as the second input to the AQDS; and

detecting a second DC offset in the output signal of the AQDS, where the second DC offset is related to a combination of DC offsets produced by the AQMS and the AQDS.

71. A circuit that digitally filters a first signal, which includes an in-phase portion and a quadrature-phase portion, to a second signal, which also includes an in-phase portion and a quadrature phase portion, the circuit comprising:

5 means for applying a first impulse response to the in-phase portion of the first signal to produce an II signal;

means for applying a second impulse response to the quadrature-phase portion of the first signal to produce a QI signal;

means for applying a third impulse response to the in-phase portion of the first signal to produce an IQ signal;

10 means for applying a fourth impulse response to the quadrature-phase portion of the first signal to produce a QQ signal;

means for combining the II signal and the QI signal to produce the in-phase portion of the second signal; and

15 means for combining the IQ signal and the QQ signal to produce the quadrature-phase portion of the second signal.

72. A circuit that calculates time domain impulse responses that complement gain and phase imbalance in a quadrature modulator, the circuit comprising:

20 means for receiving and storing at least a portion of an input signal in a memory;

means for receiving and storing at least a portion of a demodulated baseband signal in the memory;

means for analyzing the at least portions of the input signal and the demodulated baseband signal;

25 means for characterizing the quadrature impairment characteristics of an analog quadrature modulator system and an analog quadrature demodulator system in frequency domain by computing a first set of transfer functions of the quadrature impairments;

30 means for computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises an inverse system response to the first set of transfer functions;

means for converting a first portion of the second set of transfer functions to a first set of time domain impulse responses that substantially negates the gain and phase imbalance in the analog quadrature modulator system; and

5 means for converting a second portion of the second set of transfer functions to a second set of time domain impulse responses that substantially negates the gain and phase imbalance in the analog quadrature demodulator system.

73. A circuit that at least partially compensates for a gain and phase imbalance in an analog quadrature modulator system (AQMS), the circuit comprising:

10 means for applying test signals that include a plurality of baseband frequencies to a forward path of the AQMS;

means for detecting an envelope of an output signal of the AQMS;

15 means for storing at least a portion of the envelope of the output signal in a memory;

means for relating the at least portion of the envelope to the applied test signals;

20 means for characterizing the gain and phase imbalance of the AQMS in frequency domain by computing a first set of transfer functions of the quadrature impairment characteristics;

means for computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises an inverse system response to the first set of transfer functions;

25 means for converting a first portion of the second set of transfer functions to time domain impulse responses that substantially negate the gain and phase imbalance in the AQMS; and

means for applying the time domain impulse responses to input signals in the forward path of the AQMS.

74. A circuit that distinguishes gain and phase imbalances produced by an analog quadrature modulator system (AQMS) from gain and phase imbalances produced by an analog quadrature demodulator system (AQDS), the circuit comprising:

5 means for selectively applying at least three phase shifted versions of a local oscillator signal as an input to the AQDS;

means for monitoring and storing at least a portion of a first signal that is upstream of the AQMS and at least a portion of a second signal that is downstream of the AQDS for at least three of the phase shifted versions selected; and

10 means for computing a frequency domain transfer function of the AQMS and the AQDS gain and phase imbalances.